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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,722	07/10/2003	Si Bum Kim	29936/39463	2678

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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,722	KIM, SI BUM	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/6/2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/5/2005, 5/27/200*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

In view of Applicant's amendment to the specification, the objections are withdrawn.

In view of Applicant's amendment to claim 1, the objections are withdrawn.

In view of Applicant's cancellation of the claims, the rejections of claims 7 and 14 under 35 U.S.C. 112 first paragraph are rendered moot.

In view of Applicant's arguments and the amendments to the claims, the rejections of claims 6 and 13 under 35 U.S.C. 112 second paragraph, as being indefinite, are withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, and 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art (AAPA, see Figures 1 and 2 and pages 1-3 of the specification) in view of Ho et al. (U.S. Patent Appl. 2002/0115283) and Chou et al. (U.S. Patent No. 6,706,166).

In re claim 1, AAPA discloses a method of forming a copper wiring in a semiconductor device the method comprising:

forming damascene patterns (12) in an interlayer insulating film which is formed on a substrate;

sequentially forming a copper barrier metal layer (13) and a copper seed layer (14) on the surface of the interlayer insulating film including the damascene patterns;

performing a copper electroplating process (see Specification, page 2, lines 17-21) to be filled the damascene patterns with a copper layer;

and polishing the copper layer, the copper seed layer and the copper barrier metal layer by means of a chemical mechanical polishing process so that the surface of the interlayer insulating film is exposed, thereby forming copper wirings within the damascene patterns (see specification, page 2, lines 22-25).

The AAPA does not disclose the method of polishing the copper layer by means of a copper electro-polishing process to form a polished copper layer having a flat surface and a thin thickness; and polishing thereafter by means of a chemical mechanical polishing process so that the surface of the interlayer insulating film is exposed, thereby forming copper wirings within the damascene patterns.

Ho et al. disclose the method of polishing the copper layer by means of a copper electro-polishing process to form a polished copper layer having a flat surface and a thin thickness; and polishing thereafter by means of a chemical mechanical polishing process so that the surface of the interlayer insulating film is exposed, thereby forming copper wirings within the damascene patterns (see [0036]-[0039]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to planarize the copper layer by means of a copper electro-polishing process to form a polished copper layer having a flat surface and a thin thickness; and polishing thereafter by means of a chemical mechanical polishing process because as Ho et al. teaches it prevents the problems of defects caused by mechanical scratches, chemical corrosion, and oxidation of components (see [0025] and [0014]).

The AAPA nor Ho et al. disclose the method of utilizing a single apparatus to perform the electroplating and electro polishing by changing the negative power supply to a positive power supply. Chou et al. discloses utilizing a single apparatus to perform an electroplating process and an electro polishing process by changing the negative power supply to a positive power supply (see column 2 lines 43 through column 3, lines 12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a single apparatus to perform both the electroplating and electro polishing in order to reduce capital costs and risk of contamination from transfer of the wafer from one apparatus to another.

In re claim 2, AAPA disclose the method wherein the copper barrier metal layer is formed using one of ionized PVD TiN, CVD TiN, MOCVD TiN, ionized PVD Ta, ionized PVD TaN, CVD Ta, CVD TaN and CVD WN (see page 2, lines 10-15).

In re claim 3, AAPA disclose the method wherein the copper seed layer is formed using an ionized PVD method (see page 2, lines 10-15).

In re claim 4 and 5, AAPA disclose the method as claimed in claim 1, wherein the copper electroplating process comprises: loading the substrate on which the copper seed layer is formed onto an electroplating apparatus in which a copper plating solution including an organic accelerator an organic suppressor and an organic leveler are added and setting a plating target range so that the damascene patterns could be sufficiently filled; and applying the negative (-) power supply with current to the substrate (see Specification, page 2, lines 22-25, and page 3, lines 18-20 and Figures 1 and 2).

The AAPA does not disclose the negative power supply has a current in the range of 1 to 5 A. The examiner notes that Applicant does not teach that the current range solves any stated problem or is for any particular purpose. Therefore, the current range lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the electroplating at a current range of 1-5 A, since the invention would perform equally well with a different current range than the claimed range as long as it is sufficient to allow for electroplating and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 6 the combined AAPA and Ho et al. disclose the method setting a target polishing thickness equal to a thickness of the copper layer (see Ho et al.,

[0037]) 3d and 3e) and the method wherein a positive (+) power supply is applied to the wafer for electro-polishing (see [0037] anode).

AAPA and Ho et al. do not disclose the method wherein during the electro-polishing a current in the range of 1 - 30A is applied to the wafer. The examiner notes that Applicant does not teach that the current range or the target range solve any stated problem or are for any particular purpose. Therefore, the current range and the target range lack criticality in the claimed invention and do not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the electro-polishing at a current range of 1-30 A, since the invention would perform equally well with a different current range than the claimed range as long as it is sufficient to allow for electro-polishing and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to set the target range similar to a target plating range for forming the copper layer so that the same target and equipment may be used for both the electroplating and the electro-polishing and since the invention would perform equally well with a different target range than the claimed range as long as it is sufficient to allow for electro-polishing because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 8, AAPA discloses a method of forming a copper wiring in a semiconductor device the method comprising:

forming damascene patterns (12) in an interlayer insulating film which is formed on a substrate;

sequentially forming a copper barrier metal layer (13) and a copper seed layer (14) on the surface of the interlayer insulating film including the damascene patterns;

performing a copper electroplating process (see Specification, page 2, lines 17-21) to be filled the damascene patterns with a copper layer; and

polishing the copper barrier metal layer by means of a chemical mechanical polishing process until the surface of the interlayer insulting film is exposed patterns (see specification, page 2, lines 22-25).

The AAPA does not disclose the method of polishing the copper layer and the copper seed layer by means of a copper electro-polishing process until the copper barrier metal layer is exposed, thereby forming copper wirings within the damascene pattern.

Ho et al. disclose the method of polishing a copper layer by means of a copper electro-polishing process until the copper barrier metal layer is exposed, thereby forming copper wirings within the damascene pattern; and polishing thereafter by means of a chemical mechanical polishing process so that the surface of the interlayer insulating film is exposed, thereby forming copper wirings within the damascene patterns (see [0036]-[0039]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to planarize the copper layer by means of a copper electro-polishing process; and polishing thereafter by means of a chemical mechanical polishing process because as Ho et al. teaches it prevents the problems of defects caused by mechanical scratches, chemical corrosion, and oxidation of components (see [0025] and [0014])

The examiner notes that in the combined AAPA and Ho et al. process, the copper layer of Ho et al. would include the copper seed layer and the bulk copper layer of AAPA, and thus both the copper seed layer and the copper layer, would be electro-polished.

The AAPA nor Ho et al. disclose the method of utilizing a single apparatus to perform the electroplating and electro polishing by changing the negative power supply to a positive power supply. Chou et al. discloses utilizing a single apparatus to perform an electroplating process and an electro polishing process by changing the negative power supply to a positive power supply (see column 2 lines 43 through column 3, lines 12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a single apparatus to perform both the electroplating and electro polishing in order to reduce capital costs and risk of contamination from transfer of the wafer from one apparatus to another

In re claim 9, AAPA disclose the method wherein the copper barrier metal layer is formed using one of ionized PVD TiN, CVD TiN, MOCVD TiN, ionized PVD Ta, ionized PVD TaN, CVD Ta, CVD TaN and CVD WN (see page 2, lines 10-15).

In re claim 10, AAPA disclose the method wherein the copper seed layer is formed using an ionized PVD method (see page 2, lines 10-15).

In re claim 11 and 12, AAPA disclose the method as claimed in claim 1, wherein the copper electroplating process comprises: loading the substrate on which the copper seed layer is formed onto an electroplating apparatus in which a copper plating solution including an organic accelerator an organic suppressor and an organic leveler are added and setting a plating target range so that the damascene patterns could be sufficiently filled; and applying the negative (-) power supply with current to the substrate (see Specification, page 2, lines 22-25, and page 3, lines 18-20 and Figures 1 and 2).

The AAPA does not disclose the negative power supply has a current in the range of 1 to 5 A. The examiner notes that Applicant does not teach that the current range solves any stated problem or is for any particular purpose. Therefore, the current range lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the electroplating at a current range of 1-5 A, since the invention would perform equally well with a different current range than the claimed range as long as it is sufficient to allow for electroplating and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 13 the combined AAPA and Ho et al. disclose the method setting a target polishing thickness equal to a thickness of the copper layer (see Ho et al., [0037]) 3d and 3e) and the method wherein a positive (+) power supply is applied to the wafer for electro-polishing (see [0037] anode).

AAPA and Ho et al. do not disclose the method wherein during the electro-polishing a current in the range of 1 - 30A is applied to the wafer. The examiner notes that Applicant does not teach that the current range or the target range solve any stated problem or are for any particular purpose. Therefore, the current range and the target range lack criticality in the claimed invention and do not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the electro-polishing at a current range of 1-30 A, since the invention would perform equally well with a different current range than the claimed range as long as it is sufficient to allow for electro-polishing and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to set the target range similar to a target plating range for forming the copper layer so that the same target and equipment may be used for both the electroplating and the electro-polishing and since the invention would perform equally well with a different target range than the claimed range as long as it is sufficient to allow for electro-polishing because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering

the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

Claims 1-6, and 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art (AAPA, see Figures 1 and 2 and pages 1-3 of the specification) in view of Ho et al. (U.S. Patent Appl. 2002/0115283) and Talieh (U.S. Patent No. 6,176,992).

In re claim 1, AAPA discloses a method of forming a copper wiring in a semiconductor device the method comprising:

forming damascene patterns (12) in an interlayer insulating film which is formed on a substrate;

sequentially forming a copper barrier metal layer (13) and a copper seed layer (14) on the surface of the interlayer insulating film including the damascene patterns;

performing a copper electroplating process (see Specification, page 2, lines 17-21) to be filled the damascene patterns with a copper layer;

and polishing the copper layer, the copper seed layer and the copper barrier metal layer by means of a chemical mechanical polishing process so that the surface of the interlayer insulating film is exposed, thereby forming copper wirings within the damascene patterns (see specification, page 2, lines 22-25).

The AAPA does not disclose the method of polishing the copper layer by means of a copper electro-polishing process to form a polished copper layer having a flat surface and a thin thickness; and polishing thereafter by means of a chemical

mechanical polishing process so that the surface of the interlayer insulating film is exposed, thereby forming copper wirings within the damascene patterns.

Ho et al. disclose the method of polishing the copper layer by means of a copper electro-polishing process to form a polished copper layer having a flat surface and a thin thickness; and polishing thereafter by means of a chemical mechanical polishing process so that the surface of the interlayer insulating film is exposed, thereby forming copper wirings within the damascene patterns (see [0036]-[0039]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to planarize the copper layer by means of a copper electro-polishing process to form a polished copper layer having a flat surface and a thin thickness; and polishing thereafter by means of a chemical mechanical polishing process because as Ho et al. teaches it prevents the problems of defects caused by mechanical scratches, chemical corrosion, and oxidation of components (see [0025] and [0014]).

The AAPA nor Ho et al. disclose the method of utilizing a single apparatus to perform the electroplating and electro polishing by changing the negative power supply to a positive power supply. Talieh discloses utilizing a single apparatus to perform an electroplating process and an electro polishing process by changing the negative power supply to a positive power supply (see column 4 lines 60 through column 5, lines 32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a single apparatus to perform both the electroplating and electro

polishing in order to reduce capital costs and risk of contamination from transfer of the wafer from one apparatus to another.

In re claim 2, AAPA disclose the method wherein the copper barrier metal layer is formed using one of ionized PVD TiN, CVD TiN, MOCVD TiN, ionized PVD Ta, ionized PVD TaN, CVD Ta, CVD TaN and CVD WN (see page 2, lines 10-15).

In re claim 3, AAPA disclose the method wherein the copper seed layer is formed using an ionized PVD method (see page 2, lines 10-15).

In re claim 4 and 5, AAPA disclose the method as claimed in claim 1, wherein the copper electroplating process comprises: loading the substrate on which the copper seed layer is formed onto an electroplating apparatus in which a copper plating solution including an organic accelerator an organic suppressor and an organic leveler are added and setting a plating target range so that the damascene patterns could be sufficiently filled; and applying the negative (-) power supply with current to the substrate (see Specification, page 2, lines 22-25, and page 3, lines 18-20 and Figures 1 and 2).

The AAPA does not disclose the negative power supply has a current in the range of 1 to 5 A. The examiner notes that Applicant does not teach that the current range solves any stated problem or is for any particular purpose. Therefore, the current range lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the electroplating at a current range of 1-5 A,

since the invention would perform equally well with a different current range than the claimed range as long as it is sufficient to allow for electroplating and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 6 the combined AAPA and Ho et al. disclose the method setting a target polishing thickness equal to a thickness of the copper layer (see Ho et al., [0037]) 3d and 3e) and the method wherein a positive (+) power supply is applied to the wafer for electro-polishing (see [0037] anode).

AAPA and Ho et al. do not disclose the method wherein during the electro-polishing a current in the range of 1 - 30A is applied to the wafer. The examiner notes that Applicant does not teach that the current range or the target range solve any stated problem or are for any particular purpose. Therefore, the current range and the target range lack criticality in the claimed invention and do not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the electro-polishing at a current range of 1-30 A, since the invention would perform equally well with a different current range than the claimed range as long as it is sufficient to allow for electro-polishing and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A. Further, it would have been obvious to one

of ordinary skill in the art at the time the invention was made to set the target range similar to a target plating range for forming the copper layer so that the same target and equipment may be used for both the electroplating and the electro-polishing and since the invention would perform equally well with a different target range than the claimed range as long as it is sufficient to allow for electro-polishing because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 8, AAPA discloses a method of forming a copper wiring in a semiconductor device the method comprising:

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The AAPA does not disclose the method of polishing the copper layer and the copper seed layer by means of a copper electro-polishing process until the copper

barrier metal layer is exposed, thereby forming copper wirings within the damascene pattern.

Ho et al. disclose the method of polishing a copper layer by means of a copper electro-polishing process until the copper barrier metal layer is exposed, thereby forming copper wirings within the damascene pattern; and polishing thereafter by means of a chemical mechanical polishing process so that the surface of the interlayer insulating film is exposed, thereby forming copper wirings within the damascene patterns (see [0036]-[0039]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to planarize the copper layer by means of a copper electro-polishing process; and polishing thereafter by means of a chemical mechanical polishing process because as Ho et al. teaches it prevents the problems of defects caused by mechanical scratches, chemical corrosion, and oxidation of components (see [0025] and [0014])

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supply to a positive power supply (see column 4 lines 60 through column 5, lines 32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a single apparatus to perform both the electroplating and electro polishing in order to reduce capital costs and risk of contamination from transfer of the wafer from one apparatus to another.

In re claim 9, AAPA disclose the method wherein the copper barrier metal layer is formed using one of ionized PVD TiN, CVD TiN, MOCVD TiN, ionized PVD Ta, ionized PVD TaN, CVD Ta, CVD TaN and CVD WN (see page 2, lines 10-15).

In re claim 10, AAPA disclose the method wherein the copper seed layer is formed using an ionized PVD method (see page 2, lines 10-15).

In re claim 11 and 12, AAPA disclose the method as claimed in claim 1, wherein the copper electroplating process comprises: loading the substrate on which the copper seed layer is formed onto an electroplating apparatus in which a copper plating solution including an organic accelerator an organic suppressor and an organic leveler are added and setting a plating target range so that the damascene patterns could be sufficiently filled; and applying the negative (-) power supply with current to the substrate (see Specification, page 2, lines 22-25, and page 3, lines 18-20 and Figures 1 and 2).

The AAPA does not disclose the negative power supply has a current in the range of 1 to 5 A. The examiner notes that Applicant does not teach that the current range solves any stated problem or is for any particular purpose. Therefore, the current range lacks criticality in the claimed invention and does not produce unexpected or

novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the electroplating at a current range of 1-5 A, since the invention would perform equally well with a different current range than the claimed range as long as it is sufficient to allow for electroplating and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 13 the combined AAPA and Ho et al. disclose the method setting a target polishing thickness equal to a thickness of the copper layer (see Ho et al., [0037]) 3d and 3e) and the method wherein a positive (+) power supply is applied to the wafer for electro-polishing (see [0037] anode).

AAPA and Ho et al. do not disclose the method wherein during the electro-polishing a current in the range of 1 - 30A is applied to the wafer. The examiner notes that Applicant does not teach that the current range or the target range solve any stated problem or are for any particular purpose. Therefore, the current range and the target range lack criticality in the claimed invention and do not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the electro-polishing at a current range of 1-30 A, since the invention would perform equally well with a different current range than the claimed range as long as it is sufficient to allow for electro-polishing and because it has been held that where the general conditions of a claim are disclosed in the prior art,

discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to set the target range similar to a target plating range for forming the copper layer so that the same target and equipment may be used for both the electroplating and the electro-polishing and since the invention would perform equally well with a different target range than the claimed range as long as it is sufficient to allow for electro-polishing because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

Response to Arguments

Applicant's arguments with respect to claims 1-6 and 8-13 have been considered but are moot in view of the new ground(s) of rejection. The examiner notes that Applicant has argued that Ho et al. method called electro-dissolution that includes a combination of CMP that is merely assisted by current. The examiner notes that the method of Ho et al. is an electro-polishing method since the polishing is done, at least in part, with an electrolytic solution and application of current.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Primary Examiner
Art Unit 2812

jmk